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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,920	09/11/2003	Raymond S. Tetrick	884.A31US2	6016
21186	7590 09/17/2004		EXAMINER	
SCHWEGI	MAN, LUNDBERG, WO	BRAGDON, REGINALD GLENWOOD		
P.O. BOX 2938 MINNEAPOLIS, MN 55402			ART UNIT	PAPER NUMBER
MININEAL	7E15, WIIV 33402	2188		
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Please find below and/or attached an Office communication concerning this application or proceeding.



	Application No.	Applicant(s)			
		TETRICK, RAYMOND			
Office Action Summary	10/659,920				
Office Action Summary	Examiner	Art Unit			
	Reginald G. Bragdon	2188			
The MAILING DATE of this communication Period for Reply	ation appears on the cover sheet with	n the correspondence address			
A SHORTENED STATUTORY PERIOD FOR THE MAILING DATE OF THIS COMMUNIC - Extensions of time may be available under the provisions of after SIX (6) MONTHS from the mailing date of this communication of the period for reply specified above is less than thirty (30). If NO period for reply is specified above, the maximum statused for the period for reply within the set or extended period for reply within the set or exten	ATION. 37 CFR 1.136(a). In no event, however, may a repication. days, a reply within the statutory minimum of thirty totry period will apply and will expire SIX (6) MONT III. by statute, cause the application to become ABA	oly be timely filed (30) days will be considered timely. HS from the mailing date of this communication. NDONED (35 U.S.C. § 133).			
Status					
1) Responsive to communication(s) filed	on 17 November 2003.				
·	This action is FINAL . 2b) \boxtimes This action is non-final.				
/ 					
closed in accordance with the practice					
Disposition of Claims					
4) ☐ Claim(s) 21-40 is/are pending in the a 4a) Of the above claim(s) is/are 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 21-40 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction	e withdrawn from consideration.				
9)☐ The specification is objected to by the	Examiner.				
10) The drawing(s) filed on is/are:	a)□ accepted or b)□ objected to b	y the Examiner.			
Applicant may not request that any objecti	ion to the drawing(s) be held in abeyand	ce. See 37 CFR 1.85(a).			
Replacement drawing sheet(s) including the sath or declaration is objected to I		, .			
Priority under 35 U.S.C. § 119					
_	ocuments have been received. ocuments have been received in Ap f the priority documents have been r al Bureau (PCT Rule 17.2(a)).	oplication No received in this National Stage			
Attachment(s)					
1) Notice of References Cited (PTO-892)		ummary (PTO-413)			
 Notice of Draftsperson's Patent Drawing Review (PTO 3) Information Disclosure Statement(s) (PTO-1449 or Paper No(s)/Mail Date 		/Mail Date formal Patent Application (PTO-152) 			

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DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received 17 November 2003 has been considered. Please see the attached PTO-1449(s).

Drawings

2. The drawings filed on 11 September 2003 have been approved by the Examiner.

Specification

3. Applicant is requested to update any data (continuation serial number, patent number, etc...) concerning co-pending or related applications listed in the specification.

The status of the parent application on page 1 should be updated.

Claim Objections

4. Claims 22 and 30 are objected to because of the following informalities:

As per claim 22, line 2, --an-- should be added before "additional".

As per claim 30, line 2, "or" should be --of--.

Appropriate correction is required.

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Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1, 4-5, 11, 16-17, and 20 of U.S. Patent 6,622,212 contain every element of claims 21-40 of the instant application and as such anticipates claims 21-40 of the instant application.

Claims 21-22 and 24 correspond to claim 11.

Claim 23 corresponds to claim 16.

Claim 25 corresponds to claim 20.

Claim 26-27 correspond to claim 17.

Claims 28-31 correspond to claim 11.

Claims 32-33 correspond to claim 17.

Claims 34 and 37-39 correspond to claim 1.

Claims 35-36 and 40 correspond to claim 4.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at

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uspQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 112

- 7. The following is a quotation of the first paragraph of 35 U.S.C. 112:
 - The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 8. Claim 25 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Let the preceding address be represented by the value X and the length of a preceding data block by L. The predicted address begins at a location "that immediately follows" the preceding address (X+1), "plus a length of a preceding data block" (X+1+L), "plus 1" (X+1+L+1). However, it is not clear where Applicant has support for accessing as the predicted value X+2+L.

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Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 10. Claims 21-24, 26-32, and 34-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Macon, Jr. et al. (5,600,817).

As per claim 21, Macon, Jr. et al. teaches a read-ahead ("prefetch") process for a mass storage ("input/output device") system. A portion of a cache in the main memory (DCACHE 7) is set aside as a "Most Recently Read-Ahead Section" or MRRS. The system includes a file system 10 ("I/O control circuit"), which may be embodied in hardware or software. See column 4, lines 43-51. The file system includes read-ahead functionality (Length 16, COMP 14, Address 12, and CONT 18) ("a prefetch circuit to prefetch a data block into the memory in advance of a subsequent read from the I/O device"). The address value A1 represents the "preceding address" upon which the predicted prefetch address is based (in that the read precedes the prefetching). See column 7, lines 30-32. The address value A2 (derived from A1+L, the number of units to prefetch value) represents the "predicted address", and data is prefetched for this address value. See column 7, lines 32-34. The address value A2 is stored in the MRRS. See column 7, line 36. When an next address is "demanded", the address is compared to the address (in this case A2) associated with the MRRS ("wherein the subsequent read is tracked to determine if the subsequent read reads from the predicted address"). See column 5, lines 11-17, and column 7, lines 37-39.

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As per claim 22, CONT 18 represents a state machine, and it performs the function of updating, or adjusting, the MRRS value and the length 16 value. See column 5, lines 20-47.

As per claim 23, the read ahead functionality is located within the file system 10 which corresponds to the claimed "I/O control circuit" as detailed above.

As per claim 24, the file system, in which the read ahead functionality resides, is an interface for main memory 3, CPU 2, and mass storage 4.

As per claim 26, Macon, Jr. et al. teaches, with reference to figure 6, that as long as there is a first hit in the MRRS (step "B", where the address value in the MRRS is the predicted address and a hit represents the demand address matching the address in the MRRS as set forth in column 5, lines 48-50), then prefetching of a number L of units continues (step "G").

As per claim 27, Macon, Jr. et al. teaches, with reference to figure 6, that if there is a MRRS miss (i.e. the demand address does not match the value in the MRRS) and a DCACHE hit (step "I"), no prefetching occurs (processing goes to step "O").

As per claim 28, Macon, Jr. et al. teaches a CPU 2 ("a processor") and a mass storage 4 ("an Input/Output (I/O) device"). The system includes a file system 10, which may be embodied in hardware or software. See column 4, lines 43-51. The file system includes read-ahead functionality (Length 16, COMP 14, Address 12, and CONT 18). The address value A1 represents the "preceding address" upon which the predicted prefetch address is based (in that the read precedes the prefetching). See column 7, lines 30-32. The address value A2 (derived from A1+L, the number of units to prefetch value) is used to prefetch data ("the prefetch interface predicts an address needed within the I/O device to satisfy the request"). See column 7, lines 32-34. The address value A2 is stored in the MRRS. See column 7, line 36. When an

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next address is "demanded", the address is compared to the address (in this case A2) associated with the MRRS ("the prefetch interface tracks its performance"). See column 5, lines 11-17, and column 7, lines 37-39. Macon, Jr. et al. teaches, with reference to figure 6, that as long as there is a first hit in the MRRS (step "B", where the address value in the MRRS is the predicted address and a hit represents the demand address matching the address in the MRRS as set forth in column 5, lines 48-50), then prefetching of a number L of units continues (step "G") ("biases in favor...prefetching additional data in advance of subsequent requests based on success rates"). Macon, Jr. et al. further teaches, with reference to figure 6, that if there is a MRRS miss (i.e. the demand address does not match the value in the MRRS) and a DCACHE hit (step "I"), no prefetching occurs (processing goes to step "O") ("biases...against prefetching additional data in advance of subsequent requests based on success rates").

As per claim 29, Macon, Jr. et al. teaches that the entire address value in the MRRS must match the demand value (column 5, lines 48-50). Therefore, "at least a portion of the prefetched data" satisfies the request.

As per claim 30, as set forth in figure 6, the prefetching is configured to adjust whether or not to prefetch, and how much to prefetch (the L value) based on hits or misses in the MRRS and Dcache.

As per claim 31, CONT 18 represents a state machine, and it performs the function of updating, or adjusting, the MRRS value and the length 16 value. See column 5, lines 20-47.

As per claim 32, CONT 18 controls whether prefetching occurs (i.e. step G of figure 6 is performed) or does not occur (step G is not performed). See figure 6.

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As per claim 34, this claim is rejected for the reasons set forth for claim 28, above, noting that the "success" rate is based on a hit or miss of the value in the MRRS register as compared to the demand value.

As per claim 35, this claim is rejected for the reasons set forth for claim 27, above.

As per claim 36, this claim is rejected for the reasons set forth for claim 26, above.

As per claims 37-38, the address value A1 represents the "prior read request" upon which the predicted prefetch address is based (in that the read precedes the prefetching).

As per claim 39, Macon, Jr. et al. teaches that the entire address value in the MRRS must match the demand value (column 5, lines 48-50). Therefore, "at least a portion of the prefetched data" satisfies the request.

As per claim 40, CONT 18 represents a state machine, and it performs the function of updating, or adjusting, the MRRS value and the length 16 value. See column 5, lines 20-47.

Conclusion

11. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at (703) 872-9306:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at (703) 746-5693 (after October 14, 2004, the "INFORMAL" or "DRAFT" FAX number will be 571-273-4204), only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

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12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823 (after October 14, 2004, the telephone number will be 571-272-4204). The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903 (after October 14, 2004, the telephone number will be 571-272-4210).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

RGB September 16, 2004 Reginald G. Bragdon Primary Patent Examiner Art Unit 2188

Reguell D. Brogdon